Customer No.: 31561
Application No.: 10/064,078
Docket No.: 7050-US-PA

REMARKS

Present Status of the Application

The Office Action rejected all presently pending claims 1-11. Specifically, the Office Action rejected claims 1-2 and 5-6 under 35 U.S.C. 102(b), as being anticipated by Van Veen et al. (US Patent 5,801,485). The Office Action also rejected claims 1-4 and 6-11 under 35 U.S.C. 102(b) as being unpatentable over Tjanden et al. (US Patent 6,012,958). Applicants have amended claims 1and 7 to recite the feature of the present invention more clearly. After entry of the foregoing amendments, claims 1-11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1-2 and 5-6 under 35 U.S.C. 102(b), as being anticipated by Van Veen et al. (US Patent 5,801,485). Also, the Office Action rejected claims 1-4 and 6-11 under 35 U.S.C. 102(b), as being anticipated by Tjanden et al. (US Patent 6,012,958). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Independent claims 1 and 7 recite the features as follows:

1. (currently amended) A field emission display, comprising:

a cathode substrate;
a plurality of column lines on the cathode substrate;
a resistance layer, covering the column lines;
a plurality of gate row lines across the column lines;
an insulation layer under the gate row lines to isolate the gate row lines, wherein the gate row lines and the insulation layer have a plurality of openings therein to expose a portion of the resistance layers, ***and the insulation layer further has a plurality of trenches between the gate row lines to exposes a portion of the resistance layer*** ;
a plurality of micro-tips on the resistance layer in the openings to generate electrons; and
an anode substrate, located on the gate row lines to construct a vacuum space between the anode substrate and the cathode substrate.

(emphasis added).

7. (currently amended) A cathode of a field emission display, comprising:
a cathode substrate;
a plurality of column lines on the cathode substrate;
a resistance layer covering the column lines;
a plurality of gate row lines across the column lines;
an insulation layer located under the gate row lines for isolation, wherein ***the gate row lines and*** the insulation layer ***have a plurality of openings therein to expose a portion of the resistance layers, and the insulation layer further has a plurality of trenches between the gate row lines to exposes a portion of the resistance layer***; and
a plurality of micro-tips located on the exposed resistance layer in the trench to generate electrons.

(emphasis added).

Dependent claims 2-6 and 8-11 also recite the similar features.

Customer No.: 31561
Application No.: 10/064,078
Docket No.: 7050-US-PA

Regarding Van Veen et al. (US Patent 5,801,485), Van Veen et al. do not disclose that the insulating layer ***has a plurality of trenches between the gate row lines to exposes a portion of the resistance layer***. The insulating layer 4 disclosed by Van Veen et al. merely have a plurality of openings, which field emitters 6 (FIG. 5) are formed therein. Therefore, Applicants consider that Van Veen et al. fail to disclose all the elements claimed in claim 1.

Regarding Tjanden et al. (US Patent 6,012,958), Tjanden et al. do not disclose that the insulating layer ***has a plurality of trenches between the gate row lines to exposes a portion of the resistance layer***. The insulating layer 122 (FIG. 7a) disclosed by Tjanden et al. merely have a plurality of openings, which micropoint tips 6 (FIG. 7a) are formed therein. Therefore, Applicants consider that Tjanden et al. also fail to disclose all the elements claimed in claims 1 and 7.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 7 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-6 and 8-11 patently define over the prior art as well.

Customer No.: 31561
Application No.: 10/064,078
Docket No.: 7050-US-PA

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Feb. 20, 2004

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw